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REMARKS

This paper responds to the Office action in the above-entitled application, mailed on January 20, 2006, and allowing three months for a response. This response is timely because it is being filed within the period set for response.

The present application includes pending claims 1 - 33. Claims 1, 2, 11, and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Davis et al. ("Davis") in view of Baker et al. ("Baker"). Claims 13–15 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Davis in view of Ando et al. ("Ando"). Claims 19, 20, 27, and 28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Davis in view of Baker. Claims 29–33 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Davis in view of Baker, and further in view of Ando. Claims 3, 5–10, 16–18, and 20–26 stand rejected under official notice.

The Applicants will address all the points raised by the Examiner and demonstrate that the present invention is patentable. The Applicants respectfully traverse these rejections at least for the reasons discussed below.

I. Claims 1, 2, 11, and 12 Are Not Unpatentable Over Davls In View of Baker

The Applicant has been asked to show that claims 1, 2, 11, and 13 in this case are non-obvious in view of the Davis and Baker references. The applicant respectfully submits that these claims are non-obvious, for the reasons provided below.

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With regard to an obviousness rejection, Section 2142 of the MPEP states:

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

§ 2142 MANUAL OF PATENT EXAMINING PROCEDURE, 8th ed., Rev. 1 (Feb. 2003) [MPEP], Ch. 2100, p.124.

To reject claims in an application under section 103, an examiner must show an un rebutted *prima facie* case of obviousness. See In re Deuel, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper *prima facie* case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

In re Rouffet, No. 97-1492, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. July 15, 1998).

"If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." § 2142 MPEP, ch. 2100, p.121.

With regard to the third criterion of MPEP § 2142 set forth above, claim 1, from which claims 2, 11, and 13 are dependent, recites "using a limited-width test bus whose

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bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers," which the Davis reference does not disclose. The rejected claims are non-obvious for this reason alone, notwithstanding the Davis reference. Claim 1 also recites "monitoring contents of at least one of a plurality of semaphore registers," which the Baker reference also does not disclose. The rejected claims are also non-obvious for this independent reason, notwithstanding the Baker reference.

Additionally, with regard to the first criterion of MPEP § 2142 set forth above, there is no teaching, suggestion, or incentive for one of ordinary skill in the art to combine the Davis and Baker references or to modify the Davis reference as the Office Action proposes, to arrive at the present invention. The Baker reference is not pertinent to the problem of a method for monitoring hardware resources by using semaphore registers addressed by the present invention. The Baker reference discloses a "technique for transmitting address information between a processor and a plurality of memory subsystems in a common bus communication system." See Baker at Abstract. No reason has been shown why it would be obvious to selectively combine these references to produce the claimed combination, particularly in view of Baker.

Obviousness cannot be established by combining pieces of prior art absent some "teaching, suggestion, or incentive supporting the combination."¹

¹ In re Geiger, 815 F.2d 686, 2 U.S.P.Q.2d 1276, 1278 (Fed Cir. 1987).

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"[V]irtually all [inventions] are combinations of old elements." Environmental Designs, Ltd. v. Union Oil Co., 713 F.2d 693, 698, 218 USPQ 865, 870 (Fed. Cir. 1983); see also Richdel, Inc. v. Sunspool Corp., 714 F.2d 1573, 1579-80, 219 USPQ 8, 12 (Fed. Cir. 1983) ("Most, if not all, inventions are combinations and mostly of old elements."). Therefore an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue.

In re Rouffet, No. 97-1492, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. July 15, 1998).

Where a combination invention can only be arrived at by combining various components described in separate prior art references, there must be some reason for the combination; a teaching, a motivation, an incentive, or a suggestion.²

The rejection depends upon the improper use of hindsight to re-create the presently claimed combination of elements. The invention is not obvious from the prior art itself. One cannot use hindsight reconstruction, picking and choosing among isolated disclosures in the prior art, to deny that the claimed invention is unobvious.³

To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would

² In re Laskowski, 871 F.2d 115, 117, 10 U.S.P.Q.2d 1397, 1398-99 (Fed. Cir. 1989).

³ In re Fine, 837 F.2d 1071, 1075, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

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select the elements from the cited prior art references for combination in the manner claimed.

In re Rouffet, No. 97-1492, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. July 15, 1998).

For at least the reasons provided, claims 1, 2, 11, and 12 are non-obvious in view of the cited prior art.

II. Claims 13-15 Are Not Unpatentable Over Davis in View of Baker and in Further View of Ando

The Applicant has been asked to show that claims 13-15 in this case are non-obvious in view of the Davis and Baker references and in further view of the Ando reference. The applicant respectfully submits that these claims are non-obvious, for at least the reasons provided below.

With regard to the third criterion of MPEP § 2142 set forth above, claim 13, from which claims 14 and 15 are dependent, recites "arranging a plurality of semaphore registers into a plurality of semaphore register blocks" which neither the Davis reference nor the Baker reference disclose. The rejected claims are non-obvious for this reason alone, notwithstanding the Davis reference or the Baker reference. Additionally, claim 13 also recites "selecting one of said plurality of semaphore register blocks to be accessed by a limited-width test bus," which the Ando reference does not disclose. The rejected claims are non-obvious for this additional independent reason, notwithstanding the Ando reference.

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Furthermore, with regard to the first criterion of MPEP § 2142 set forth above, there is no teaching, suggestion, or incentive for one of ordinary skill in the art to combine the Davis, Baker and Ando references or modify the Davis reference as the Office Action proposes, to arrive at the present invention. Again, the Baker reference is not pertinent to the problem of a method for monitoring hardware resources by using semaphore registers addressed by the present invention. In fact, neither is the Ando reference. The Ando reference discloses a "bus circuit of a precharging type [that] has an hierarchical structure comprising a higher rank bus and a plurality of lower rank buses connected in parallel thereto." See Ando at Abstract. No reason has been shown why it would be obvious to selectively combine these references to produce the claimed combination, particularly in view of Baker and in further view of Ando.

For at least the reasons provided, claims 13-15 are therefore non-obvious in view of the cited prior art.

III. Claims 19, 20, 27, and 28 Are Not Unpatentable Over Davis in View of Baker

The Applicant has been asked to show that claims 19, 20, 27, and 28 in this case are non-obvious in view of the Davis and Baker references. The applicant respectfully submits that these claims are non-obvious, for at least the reasons provided below.

With regard to the third criterion of MPEP § 2142 set forth above, claim 19, from which claims 20, 27, and 28 are dependent, recites a "limited-width test bus [that] contains less than a number of bits needed to individually address each of said plurality

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of semaphore registers," which the Davis reference does not disclose. The rejected claims are non-obvious for this reason alone, notwithstanding the Davis reference. Additionally, claim 19 also recites "a plurality of semaphore registers," which the Baker reference does not disclose. The rejected claims are non-obvious for this additional independent reason, notwithstanding the Baker reference.

Furthermore, with regard to the first criterion of MPEP § 2142 set forth above, there is no teaching, suggestion, or incentive for one of ordinary skill in the art to combine the Davis and Baker references or modify the Davis reference as the Office Action proposes, to arrive at the present invention. The Baker reference is not pertinent to the problem of a system for monitoring hardware resources by using semaphore registers addressed by the present invention. No reason has been shown why it would be obvious to selectively combine these references to produce the claimed combination, particularly in view of Baker.

For at least the reasons provided, claims 19, 20, 27, and 28 are therefore non-obvious in view of the cited prior art.

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IV. Claims 29-33 Are Not Unpatentable Over Davis in View of Baker and in Further View of Ando

The Applicant has been asked to show that claims 29-33 in this case are non-obvious in view of the Davis and Baker references and in further view of the Ando reference. The applicant respectfully submits that these claims are non-obvious, for at least the reasons provided below.

With regard to the third criterion of MPEP § 2142 set forth above, claim 29, from which claims 30-33 are dependent, recites a "plurality of semaphore register blocks" and a "selector," which neither the Davis reference nor the Baker reference discloses. The rejected claims are non-obvious for this reason alone, notwithstanding the Davis reference or the Baker reference. Additionally, claim 29 also recites "a limited-width test bus," which neither the Davis reference nor the Ando reference discloses. The rejected claims are non-obvious for this additional independent reason, notwithstanding the Davis reference or the Ando reference.

Furthermore, with regard to the first criterion of MPEP § 2142 set forth above, there is no teaching, suggestion, or incentive for one of ordinary skill in the art to combine the Davis and Baker references in further view of the Ando reference or to modify the Davis reference as the Office Action proposes, to arrive at the present invention. . Neither the Baker reference nor the Ando reference are pertinent to the problem of a system for monitoring hardware resources by using semaphore registers addressed by the present invention. No reason has been shown why it would be obvious to selectively combine

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these references to produce the claimed combination, particularly in view of Baker and in further view of Ando.

For at least the reasons provided, claims 29-33 are therefore non-obvious in view of the cited prior art.

V. Official Notice of Claims 3, 5, 6, 8-10, 16-18, and 20-26

Applicant respectfully challenges the taking of Official Notice with respect to claims 3, 5, 6, 8-10, 16-18, and 20-26 as improper. The Office Action asserts that "the use of OR/AND/XOR gates is old, and well known in the art for the purposes of determining if all of a number of bits are set to logic 1, logic 0, or if all bits are different, in a digital system." The issue is not whether individual elements in claim 3, 5, 6, 8-10, 16-18, and 20-26 are *individually* novel or non-obvious. The Examiner appears to have taken this perspective, which is erroneous. The issue is whether the *combination* of claims 3, 5, 6, 8-10 with claim 1, from which they depend, or the *combination* of claims 16-18 with claim 13, from which they depend, or the *combination* of claims 20-26 with claim 19, from which they depend, is novel or non-obvious.

In the context of the claimed invention as set forth in claim 1, the elements recited in claims 3, 5, 6, 8-10 are not well known or obvious. For example, regarding claim 3, it is non-obvious to determine whether a hardware resource is in use by monitoring contents of at least one of a plurality of semaphore registers; to access the monitored contents of the plurality of semaphore registers by using a limited-width test

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bus whose bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers; and to make that determination by ORing each register bit location in each of the plurality of semaphore registers if a protocol reset state is logic 0.

In the context of the claimed invention as set forth in claim 13, the elements recited in claims 16-18 are not well known or obvious. For example, regarding claim 16, it is non-obvious to arrange a plurality of semaphore registers into a plurality of semaphore register blocks; to select one of the plurality of semaphore register blocks to be accessed by a limited-width test bus; and to determine whether a hardware resource is in use by ORing each register bit location in each of the plurality of semaphore registers if a protocol reset state is logic 0.

In the context of the claimed invention as set forth in claim 19, the elements recited in claims 20-26 are not well known or obvious. For example, regarding claim 20, it is non-obvious to have a system that comprises a plurality of hardware resources; that also comprises a plurality of semaphore registers coupled to the plurality of hardware resources; that also comprises a limited-width test bus coupled to the plurality of semaphore registers, wherein the limited-width test bus contains less than a number of bits needed to individually address each of the plurality of semaphore registers; and where a portion of the limited-width test bus is assigned to address each of the plurality of semaphore registers and a remaining portion to address each register bit location in the plurality of semaphore registers.

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As can be seen, the elements as set forth in claims 3, 5, 6, 8-10, 16-18, and 20-26 in the respective contexts of the claimed inventions as set forth in claims 1, 13 and 19 are hardly obvious or well known. In the proper context of the respective claimed inventions, it is improper for Official Notice to be taken with respect to claims 3, 5, 6, 8-10, 16-18, and 20-26.

Applicant respectfully requests that Official Notice be withdrawn with respect to claims 3, 5, 6, 8-10, 16-18, and 20-26.

Applicant respectfully requests that, if Official Notice is maintained in the next official communication, then the Examiner should produce documentary support, not only for the claimed inventions as set forth in claims 3, 5, 6, 8-10, 16-18, and 20-26, but also for the claimed inventions in the contexts as set forth in claims 1, 13, and 19.

"It is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based." Accordingly, in order to maintain the rejection, Applicant respectfully requests that the Examiner produce references in support of the Examiner's contention or, if the Examiner is relying upon personal knowledge to support the finding of what is known in the art, then the Examiner must provide an affidavit or declaration setting forth specific factual statements and explanations to support the finding.

See, e.g., M.P.E.P. § 2144.03 and 37 C.F.R. § 1.104(d)(2).

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VI. Official Notice of Claim 7

Applicant respectfully challenges the taking of Official Notice with respect to claim 7 as improper. The Office Action asserts that "taking the complement of the values used to determine whether or not a resource is in use as recited in claim 4 would have been well known to one of ordinary skill in this art at the time of invention by applicant." The issue is not whether individual elements in claim 7 are *individually* novel or non-obvious. The Examiner appears to have taken this perspective, which is erroneous. The issue is whether the *combination* of claim 7 with claims 6 and claim 1, from which they depend, is novel or non-obvious. Claim 7 does not depend on claim 4.

In the context of the claimed invention as set forth in claim 1, the elements recited in claims 6 and 7 are not well known or obvious. In claim 7 it is non-obvious to determine whether a hardware resource is in use by monitoring contents of at least one of a plurality of semaphore registers; to access the monitored contents of the plurality of semaphore registers by using a limited-width test bus whose bus width contains less than a number of bits needed to individually address each of said plurality of semaphore registers; the determination of whether said hardware resource is in use further comprises ANDing each register bit location in each of the plurality of semaphore registers if a protocol reset state is logic 1; and if a result of the determination is logic 1, then the hardware resource is not in use and if a result of said determination is logic 0, then the hardware resource is in use.

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As can be seen, the elements as set forth in claim 7 in the respective context of the claimed invention, as set forth in claim 1 is hardly obvious or well known. In the proper context of the respective claimed invention, it is improper for Official Notice to be taken with respect to claim 7.

Applicant respectfully requests that Official Notice be withdrawn with respect to claim 7.

Applicant respectfully requests that, if Official Notice is maintained in the next official communication, then the Examiner should produce documentary support, not only for the claimed invention as set forth in claim 7, but also for the claimed invention in the context set forth in claim 1.

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CONCLUSION

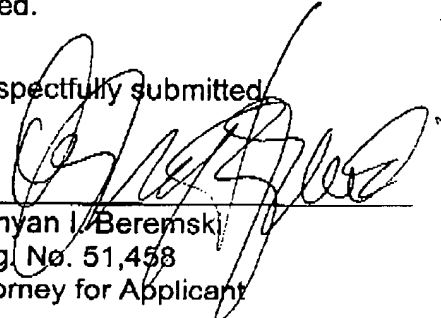
Based on at least the foregoing, the Applicant believes that all claims 1-33 are in condition for allowance. If the Examiner disagrees, the Applicant respectfully requests a telephone interview, and requests that the Examiner telephone the undersigned Attorney at (312) 775-8232.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

A Notice of Allowability is courteously solicited.

Date: April 19, 2006

Respectfully submitted,



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